Please amend claim 18 as follows:

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10. (canceled)

11. (canceled)

12. (canceled)

13. (canceled)

14. (previously presented) An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit streams of data;

a plurality of data stream processors that process the streams of data, each data

stream processor being coupled to a data stream input and/or data stream output and including

a writeable instruction memory containing instructions and

a control data processor that controls the data stream processor by sequentially executing instructions from the writeable instruction memory.

15. (previously presented) The integrated circuit set forth in claim 14 wherein:

the control data processor is a general-purpose microprocessor that has an industry-standard architecture, whereby programs for the control data processor may be developed using standard tools for the architecture.

16. (previously presented) The integrated circuit set forth in claim 14 wherein:

the streams of data include a serial stream and a parallel stream.

17. (previously presented) The integrated circuit set forth in claim 14 wherein the integrated circuit further comprises:

an aggregator that aggregates certain of the data stream processors so that the aggregated data stream processors cooperate in processing a stream of data, the aggregator including

configurable interconnections between the aggregated data stream processors;

a configurable operation coordinator that coordinates operation of the aggregated data stream processors; and

a writeable configurator that specifies the configurable interconnections and the configurable operation coordinator as required to aggregate the data stream processors.

18. (currently amended) The integrated circuit set forth in claim 14 wherein:

a data stream input and/or output includes a plurality of I/O pins that receive and/or transmit signals and

the integrated circuit further comprises:

a writeable configuration specifier for specifying a configuration of ~~the~~ a data stream inputs and/or outputs; and

configuration circuitry coupled between the plurality of I/O pins and the data

stream processor and responsive to the configuration specifier for configuring the data stream inputs and/or outputs as specified by the configuration specifier, whereby the integrated circuit may be used with a plurality of transmission protocols.

19. (previously presented) The integrated circuit set forth in claim 14 wherein each data stream processor further comprises:

a receive processor that operates under control of the control data processor to process the data stream received from the data stream input and/or

a transmit processor that operates under control of the control data processor to process the data stream for output to the data stream output.

20. (previously presented) The integrated circuit set forth in claim 19 wherein each of the receive processor or the transmit processor further comprises:

a writeable instruction memory containing instructions; and

the receive processor or the transmit processor sequentially executes certain of the instructions to process the data stream.

21. (previously presented) The integrated circuit set forth in claim 19 wherein:

the receive processor and/or the transmit processor have a plurality of processing components and are configurable to bypass one or more of the components in processing the data streams.

22. (previously presented) The integrated circuit set forth in any of claims 14 through 21 wherein the integrated circuit further comprises:

a context processor that responds to information received from a given data stream processor that is processing a data stream to produce information about the given data stream's context and provide the context information to the given data stream processor; the given data stream processor using the context information to process the data stream.

23. (previously presented) The integrated circuit set forth in any one of claims 14 through 21 wherein:

a stream of data contains control data and payload;

a received stream of data is processed in a receiving data stream processor to

extract the control data and the payload and a transmitted stream of data is processed in a transmitting data stream processor to add control data to the payload; and

the integrated circuit further comprises

a buffer manager coupled to the data stream processors that provides addresses of buffers for storing payload and responds to a write operation with a buffer address to write payload to the addressed buffer and to a read operation with a buffer address to read payload from the addressed buffer; and

a queue manager coupled to the data stream processors that manages queues of descriptors of payload, each descriptor including at least a buffer address, the queue manager responding to an enqueue command by enqueuing a descriptor provided with the command to a queue specified in the command and responding to a dequeue command by dequeuing a descriptor from the queue specified in the command,

a data stream processor responding to a received stream of data by performing a write operation to the buffer manager with the received data stream's payload and an address provided by the buffer manager and performing an enqueue operation with a descriptor containing the address and transmitting a stream of data by performing a dequeue operation, using the address in a descriptor obtained as a result of the dequeue operation in a read operation to the buffer manager, producing a data stream using the payload received from the buffer manager, and transmitting the produced data stream.